REMARKS

Claims 1, 2 and 4-16 were pending in the application. Claims 3 and 17-23 have been canceled in previous amendments. Claims 1-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Radogna et al., Latif et al. and Satou et al. Claim 15 was rejected under 35 U.S.C. §103(a) as being unpatentable over Radogna and Satou. Claims 14 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Radogna, Latif and Satou as applied to claims 1 and 15, and further in view of Muller et al. Claims 1, 2, 6 and 13-16 have been amended, and claim 4 has been canceled, leaving claims 1, 2 and 5-16 presently under consideration. A Request for Continued Examination (RCE) is being filed concurrently herewith. Reconsideration and reexamination of the application in view of the amendments and following remarks is respectfully requested.

The present invention is directed to enabling data communication between a storage area network and another network implementing a different protocol. *Two microsequencer systems* are employed to perform translations between the two different protocols. For example, *one microsequencer system* may be employed to perform a translation from a *first to a second protocol*, and *the other microsequencer system* may perform a translation from the *second to the first protocol*. Each microsequencer system may include one or more microsequencers *cooperatively connected* together to perform the translation using Very Long Instruction Words (VLIW) from an instruction memory for processing multiple instructions in parallel. Each VLIW contains a plurality of instruction fields executable in parallel by different instruction units within the microsequencer.

Claims 1-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Radogna, Latif and Satou. Claim 3 had previously been canceled, and claim4 has been canceled in this amendment, rendering the rejection moot with respect to claims 3 and 4. Claim 1 has been amended (and claims 2, 6 and 13 have also been amended to make them consistent with amended claim 1). With the amendment to claim 1, it is respectfully submitted that the rejection of claims 1, 2 and 5-13 have been overcome.

Claim 1 has been amended to recite, among other things, *first and second microsequencer systems*, the *first microsequencer system* for translating input data from a *first*

network protocol to a *second* network protocol, and the *second microsequencer system* for translating input data from a *second* network protocol to a *first* network protocol, and each microsequencer system having one or more *cooperating* microsequencers. Each of the microsequencers has access to an *instruction memory* having a plurality of VLIWs with a plurality of instruction fields executable in parallel by each of the microsequencers to enable the microsequencers to execute a plurality of instructions in a single instruction cycle.

In addition, because claims 2 and 5-13 depend from claim 1, claims 2 and 5-13 also now contain the limitations described above.

Support for the amendments to claim 1 can be found in the following locations in the specification and drawings of the present application: FIG. 2 (see first microsequencer system 24 and second microsequencer system 42), page 6 lines 20-22 and 29-30, page 7 lines 30-31, page 8 lines 5-6, FIG. 3 (see each of the first and second microsequencer systems 24 and 42 having microsequencers 47A-47E), page 8 lines 20-27, FIG. 7 (see instruction memory 118), page 9 lines 16-19 and page 18 lines 18-28.

Neither Radogna, Latif nor Satou, either alone or in combination, discloses, teaches or suggests first and second microsequencer systems for translating input data from a first network protocol to a second network protocol and vice versa, the microsequencer systems having cooperating microsequencers each having access to an instruction memory, as recited in amended claim 1.

Radogna discloses only a *single* microsequencer 100 (see FIG. 3) for performing header translation for frames being moved from an input FIFO to an output FIFO. Because Radogna is a unidirectional system, it understandably fails to disclose, teach or suggest a second microsequencer for header translation of frames being moved in the opposite direction. Furthermore, it would *not* have been obvious to one skilled in the art to simply provide another microsequencer for performing header translation for frames being moved in the opposite direction, because the invention as recited in claim 1 does not simply recite two microsequencers. Rather, claim 1 recites two microsequencer

systems with a *cooperative* relationship between microsequencers in the microsequencer systems, and that the microsequencers have *access to a common instruction memory*.

Satou also discloses only a single microsequencer. Satou is directed to a data processor that processes string operation instructions. Satou does not translate between two different network protocols in both directions, and therefore fails to disclose, teach or suggest a second microsequencer for that purpose, a cooperative relationship between microsequencers, or an instruction memory accessible by multiple microsequencers.

Latif is completely silent as to a microsequencer system of any type.

Therefore, even if one skilled in the art would have been motivated to combine Radogna, Latif or Satou, none of those references discloses, teaches or suggests first and second microsequencer systems for performing protocol conversion in both directions, or that the microsequencers in those systems cooperatively with each other and access a common instruction memory.

Because neither Radogna, Latif or Satou, alone or in combination, discloses, teaches or suggests all of the limitations of claims 1, 2 and 5-13, it is respectfully submitted that the rejection of those claims under 35 U.S.C. §103(a) as being unpatentable over Radogna, Latif and Satou has been overcome.

Claim 15 was rejected under 35 U.S.C. §103(a) as being unpatentable over Radogna and Satou. Claim 15 has been amended. With the amendment to claim 15, it is respectfully submitted that the rejection of claim 15 has been overcome.

Claim 15 has been amended to recite, among other things, *first and second processing elements*, one of the processing elements for translating input data from a *first* network protocol to a *second* network protocol, and the other processing element for translating input data from a *second* network protocol to a *first* network protocol, and each processing element having one or more *cooperating* instruction units. Each of the processing elements has access to an *instruction memory*

having a plurality of VLIWs with a plurality of instruction fields executable in parallel by each of the functional units to enable the functional units to execute a plurality of instructions in a single instruction cycle.

Support for the amendments to claim 15 can be found in the following locations in the specification and drawings of the present application: FIG. 2 (see first microsequencer system 24 and second microsequencer system 42), page 6 lines 20-22 and 29-30, page 7 lines 30-31, page 8 lines 5-6, FIG. 3 (see each of the first and second microsequencer systems 24 and 42 having microsequencers 47A-47E), page 8 lines 20-27, FIG. 7 (see instruction memory 118), page 9 lines 16-19 and page 18 lines 18-28.

As with claim 1, neither Radogna nor Satou, alone or in combination, discloses, teaches or suggests first and second processing elements for translating input data from a first network protocol to a second network protocol and vice versa, the processing elements having cooperating functional units each having access to an instruction memory, as recited in amended claim 15.

Radogna discloses only a *single* microsequencer 100 (see FIG. 3) for performing header translation for frames being moved from an input FIFO to an output FIFO. Because Radogna is a unidirectional system, it understandably fails to disclose, teach or suggest a second microsequencer for header translation of frames being moved in the opposite direction. Furthermore, it would *not* have been obvious to one skilled in the art to simply provide another microsequencer for performing header translation for frames being moved in the opposite direction, because the invention as recited in claim 15 does not simply recite two processing elements. Rather, claim 15 recites two processing elements with a *cooperative* relationship between functional units in the processing elements, and that the functional units have *access to a common instruction memory.*

Satou also discloses only a single microsequencer. Satou is directed to a data processor that processes string operation instructions. Satou does not translate between two different network protocols in both directions, and therefore fails to disclose, teach or suggest a second

microsequencer for that purpose, a cooperative relationship between microsequencers, or an instruction memory accessible by multiple microsequencers.

Therefore, even if one skilled in the art would have been motivated to combine Radogna and Satou, neither of those references discloses, teaches or suggests first and second processing elements for performing protocol conversion in both directions, or that the functional units in those processing elements cooperatively with each other and access a common instruction memory.

Because neither Radogna nor Satou, alone or in combination, discloses, teaches or suggests all of the limitations of claim 15, it is respectfully submitted that the rejection of claim 15 under 35 U.S.C. §103(a) as being unpatentable over Radogna and Satou has been overcome.

Claims 14 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Radogna, Latif and Satou as applied to claims 1 and 15, and further in view of Muller. Claim 14 depends from amended claim 1, and claim 16 depends from amended claim 15.

As described above, neither Radogna, Latif nor Satou, alone or in combination, discloses, teaches or suggests first and second microsequencer systems (or processing elements) for performing protocol conversion in both directions, or that the microsequencers (or functional units) in those systems cooperatively with each other and access a common instruction memory, as recited in amended claim 1 (or claim 15). Furthermore, Muller fails to make up for the deficiencies of Radogna, Latif and Satou.

Muller is directed to a network interface for receiving a packet from a network and transferring it to a host computer system. The header of a packet may be parsed by a *single* microsequencer located in a parser module 106 (see FIG. 1A and col. 24 lines 12-67). Muller does not translate between two different network protocols in both directions, and therefore fails to disclose, teach or suggest a second microsequencer for parsing headers in packets in a different protocol.

Therefore, even if one skilled in the art would have been motivated to combine Radogna, Latif, Satou and Muller, none of those references discloses, teaches or suggests first and second processing elements for performing protocol conversion in both directions, or that the functional units in those processing elements cooperatively with each other and access a common instruction memory, as recited in claims 1 and 15 (and therefore also claims 14 and 16).

Because neither Radogna, Latif, Satou nor Muller, alone or in combination, discloses, teaches or suggests all of the limitations of claims 14 and 16, it is respectfully submitted that the rejection of claims 14 and 16 under 35 U.S.C. §103(a) as being unpatentable over Radogna, Latif, Satou and Muller has been overcome.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If, for any reason, the Examiner finds the application other than in condition for allowance, Applicants request that the Examiner contact the undersigned attorney at the Los Angeles telephone number (213) 892-5752 to discuss any steps necessary to place the application in condition for allowance.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicants petition for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing Docket No. 491442004500.

Dated: June 5, 2006

Respectfully submitted,

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